1. ELEC 522: Advanced VLSI Design
Rice University: Fall 2017, Abercrombie Labs AEL A116

2. Credits: 3 credit hours
Lectures: Tuesday and Thursday, 1:00 to 2:20pm AEL A116
3. Course Instructor: Joe Cavallaro , DCH 3042, cavallar@rice.edu
4. Office Hours: After class or by appointment

5. Grade Policies: Grading will be based on the projects and presentations assigned during the semester. A final exam on the text and readings may be given.

6. Absence Policies: Attendance and participation in class is expected. In general, the class on Tuesday is lecture oriented, while the class on Thursday is often focused on design tools and laboratory tutorials.

7. Textbook and Course Materials:

- Wayne Wolf, FPGA-Based System Design, Prentice Hall, 2004, ISBN 0-13-142461-0
  Emphasis on Chapters 1, 3, 6, 7 (about 250 pages). http://www.amazon.com/FPGA-Based-System-Design-Prentice-Semiconductor/dp/0131424610/ref=sr_1_3/102-0171952-4496933?ie=UTF8&s=books&qid=1188319895&sr=1-3
- Walter Tuttlebee, Editor, Software Defined Radio, Baseband Technology for 3G Handsets and Basestations, John Wiley and Sons, 2004, ISBN 0-470-86770-1
  Emphasis on Chapters 1, 2, 3, 4, 5, 6, 7, 10, 11. (about 250 pages). http://www.amazon.com/Software-Defined-Radio-Technologies-Basestations/dp/0470867701/ref=sr_1_2/102-0171952-4496933?ie=UTF8&s=books&qid=1188320142&sr=1-2
- Louise Crockett, Ross Elliot, Martin Enderwitz, Bob Stewart, The Zynq Book, Embedded Processing with the ARM Cortex-A9 on the Xilinx Zynq-7000 All Programmable SoC, Strathclyde Academic Media, 2014, ISBN-13: 978-0-9929787-0-9 E-Book available for download from: http://www.zynqbook.com/

Other supplemental materials: Current papers and design tool tutorials posted to Owlspace
Papers (from IEEE Explore) are on ASIP design, and example architectures, (about 100 pages) including:

- From ASIC to ASIP: The Next Design Discontinuity
- Approaches to Low-Power Implementations of DSP Systems
- Custom-Instruction Synthesis for Extensible-Processor Platforms
- Issues and Approaches to Coarse-Grain Reconfigurable Architecture Development
- Design of Transport Triggered Architectures
- Design of Transport Triggered Architecture Processor for Discrete Cosine Transform
- Immediate Optimization for Compressed Transport Triggered Architecture Instructions
- ILP Architectures: Trading Hardware for Software Complexity
- ASIP Architecture Implementation of Channel Equalization Algorithms for MIMO Systems in WCDMA Downlink
- Design Space Exploration for Real-Time Embedded Stream Processors
- Semi-Parallel Reconfigurable Architectures for Real-Time LDPC Decoding
- Rapid Scheduling of Efficient VLSI Architectures for Next-Generation HSDPA Wireless System Using Precision-C Synthesizer

8. Specific Course Information:

a. Catalog Description: Design and analysis of algorithm-specific VLSI processor architectures. Topics include the implementation of pipelined and systolic processor arrays. Techniques for mapping numerical algorithms onto custom processor arrays. Course includes design project using high-level VLSI synthesis tools.

b. Prerequisites: A course in Digital Systems Design such as ELEC 326/327. An introductory course in VLSI System Design is useful. Background in computer architecture, computer arithmetic, and signal processing is also helpful.

c. Elective Status: ELEC 522 is a graduate elective. Undergraduates may take the course as a Specialization course in Computer Engineering in consultation with their advisor

d. Projects for Fall 2017 and Presentation: Approximately 6 project assignments on ASIC and FPGA Design using the Xilinx System Generator tools, along with Xilinx Vivado tools. Some assignments will use Xilinx Platform Studio and Xilinx SDK for the Zynq chip for embedded systems, and Synopsys DC Ultra for ASIC synthesis. We will also use the Cadence SOC Encounter tools in the ASIC flow for System on Chip integration and Xilinx Vivado HLS for high level synthesis. Possible fabrication through the MOSIS service. A presentation will be given in class on several of the projects, and additional presentations of research papers will be assigned for discussion. Previous year topics have included a systolic array co-processor for matrix factorization and solution of systems of linear equations. A final exam on the text and readings may be given.

ELEC_522_Proj_1_Sysgen_Intro	ELEC_522_Proj_4_Vivado_HLS_CORDIC
ELEC_522_Proj_2_Matrix_Mult	ELEC_522_Proj_5_QR_Array
ELEC_522_Proj_3_Vivado_HLS_Matrix_Mult	ELEC_522_Proj_6_4x4_Linear_System_Solver

9 Specific Goals for the Course:

a. Outcomes: The goals of the course are to study design methodologies for application-specific processors for applications particularly in wireless communications. The course includes a design project initially targeted to an FPGA. The student will be able to specify, design, simulate, assess, and verify custom accelerators and integrate experimentally into a System on Chip (Soc) platform.

b. Course Outcomes: Related to ABET Criterion 3 a through k:
The relationships to eleven criteria are listed with 1, 2, and 3. (with 3 as most related.)

a	An ability to apply knowledge of mathematics, science, and engineering.	3
b	An ability to design and conduct experiments, as well as to analyze and interpret data.	
c	An ability to design a system, component, or process to meet desired needs.	3
d	An ability to function on multi-disciplinary teams.	1
e	An ability to identify, formulate, and solve engineering problems.	2
f	An understanding of professional and ethical responsibility.	
g	An ability to communicate effectively.	
h	The broad education necessary to understand the impact of engineering solutions in a global and societal context.	
i	A recognition of the need for, and an ability to engage in life-long learning.	
j	A knowledge of contemporary issues.	
k	An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.	3

10: Topics and Course Contents: The topics covered in this course include:

- Design methodology for ASIC and FPGA implementations
- FPGA hardware structures and fabrics
- Review of Combinational Logic, Sequential Machines, and Architecture
- High-level VLSI synthesis and design tools including Synopsys, Cadence, Mentor Graphics, with CAD algorithm overview for floorplanning, placement, and routing in ASICs.
- High-level DSP algorithm simulation and code (VHDL/Verilog) generation using Xilinx System Generator, and Xilinx Vivado HLS.
- Design and analysis of algorithm-specific VLSI processor architectures. Topics include the implementation of pipelined and systolic processor structure. Techniques for mapping numerical algorithms onto custom processor arrays, including Application Specific Instruction Processors (ASIPs).
- High-level Design frameworks for systems containing custom and general-purpose units.

- Prototyping using Xilinx System Generator, Xilinx ISE tools, Xilinx Vivado, and Xilinx FPGAs with emphasis on the Xilinx Zynq chip containing ARM core and FPGA fabric.
- Adaptive computing as a technology for reconfigurable wireless systems.
- Example architectures: Blackfin, TigerSHARC, XPP, Sandblaster, TI TCI platform, picoArray.
- Heterogeneous DSP-FPGA-ASIC processors for wireless handsets
- In some years, chips may be fabricated by MOSIS depending on project topics.

Laboratory Use:
We will use: the VLSI Lab, AL A116, in Abercrombie Labs with the Xilinx ZedBoard University Development Board which contains the Xilinx Zynq-7000 chip for the course; the Rice CLEAR Linux cluster for access to Synopsys/Cadence VLSI design tools via Xwindows using Xming/MobaXterm in addition to the laboratory PCs in AL A116; Owlspace at Rice for notes and project submission.

11. Rice Honor Code: The Honor Code will apply to both individual and small group projects. Each project/paper/presentation/exam will state the specific details.

12. Students with Disabilities: Any student with a disability requiring accommodations in this course is encouraged to contact the instructor after class or during office hours. Additionally, students will need to contact Disability Support Services in the Ley Student Center.

13. Updates: Consult the class Owlspace page for updates to information contained in the syllabus.

Joe Cavallaro Updated 22 August 2017